PENDING CLAIMS AS AMENDED

Please amend the claims as follows:

1. (Currently Amended) A system for evaluating M modulo J, where J is an integer and M is an integer expressed in binary form ($M = \sum_{i=0}^{N} \alpha_i 2^i$), where α_i is 0 or 1, and $N+1$ is ~~the~~ a number of digits in a binary word[)] comprising:

a first circuit for decomposing M into two integers A and B, wherein B = M – A, the first circuit comprising a multiplexer (M1) configured to produce $B = B_N$ on a first iteration and $B = B_i$ on subsequent iterations where $B_N = (M - \alpha_N 2^N)$ and $B_i = (M' - \alpha_i 2^i)$ and where i is an iteration counter starting with N and counting down;

a second circuit for evaluating C=A modulo J (A ~~modulo~~ J);

a third circuit for evaluating M′ = ~~(A modulo J)~~ C + B; and

a fourth circuit for outputting M′ or feeding M′ back to the first ~~means~~ circuit to evaluate M′ modulo J.

2. (Cancelled).

3. (Currently Amended) The system of Claim 1, wherein the second circuit ~~includes~~ comprises a look-up table configured to store ~~that stores~~ $C_i = 2^i$ modulo J for i = 0 to N.

4. (Currently Amended) The system of Claim 3, wherein the second circuit further includes a multiplexer ~~M2~~ (M2) that passes 0 to the third circuit when ($\alpha_i = 0$), and passes C_i when ($\alpha_i = 1$).

5. (Currently Amended) The system of Claim 1, wherein the third circuit includes an adder ~~A1~~ (A1) whose inputs are B_i and ($\alpha_i C_i$) and which passes ~~its output~~ $M' = B_i + \alpha_i C_i$ ~~($\alpha_i C_i$)~~ to the fourth circuit.

6. (Currently Amended) The system of Claim 1, wherein the fourth circuit includes a multiplexer ~~M4~~ (M4) that passes M′ as a final output if (M′ < J); otherwise i is set to i-1, and M′ is fed back to the first circuit.

7. (Currently Amended) The system of Claim 1, wherein the circuit further includes fifth circuit for ensuring convergence by passing J when a bitwise AND of M′ and J equals J, otherwise passing 0.

8. (Currently Amended) The system of Claim 7, wherein the fifth circuit ~~includes~~ comprises a multiplexer ~~M3~~ (M3) that passes J when the bitwise AND of M′ and J equals J, and otherwise ~~it~~ passes 0.

9. (Currently Amended) The system of Claim 8, wherein the output of the multiplexer ~~M3~~ (M3) is subtracted from M′ by an adder A2 and the result is passed to the fourth circuit.

10. (Currently Amended) A deinterleaver comprising:

a demultiplexer;

a multiplexer; and

a circuit for connecting the outputs of the demultiplexer to the inputs of the multiplexer, wherein the circuit ~~includes a system for evaluating M modulo J comprising~~ comprises:

a first circuit for decomposing M into two integers A and B, where B = M – A;

a second circuit for evaluating (A modulo J);

a third circuit for evaluating M′ = (A modulo J) + B; and

a fourth circuit for outputting M′ or feeding M′ back to the first circuit to evaluate M′ modulo J.

Claims 11-18 (Cancelled).

19. (New) A system for evaluating M modulo J, where J is an integer and M is an integer expressed in binary form ($M = \sum_{i=0}^{N} \alpha_i 2^i$), where α_i is 0 or 1, and $N+1$ is the number of digits in a binary word comprising:

a first circuit for decomposing M into two integers A and B, wherein B = M – A;

a second circuit for evaluating C= A modulo J (A mod J) comprising a look-up table configured to store $C_i = 2^i$ modulo J for i = 0 to N and a multiplexer (M2);

a third circuit for evaluating M′ = A modulo J (A mod J) + B, the third circuit receiving 0 from the multiplexer (M2) when ($\alpha_i = 0$) and receiving C_i from the multiplexer (M2) when ($\alpha_i = 1$); and

a fourth circuit for outputting M′ or feeding M′ back to the first circuit to evaluate M′ modulo J.

20. (New) A system in accordance with claim 19, wherein the first circuit comprises:

a multiplexer (M1) configured to pass B to the second circuit where $B = B_N = (M - \alpha_N 2^N)$ on a first iteration and $B = B_i = (M' - \alpha_i 2^i)$ on all subsequent iterations and where i is an iteration counter starting with N and counting down.

21. (New) A system for evaluating M modulo J, where J is an integer and M is an integer expressed in binary form ($M = \sum_{i=0}^{N} \alpha_i 2^i$), where α_i is 0 or 1, and $N+1$ is the number of digits in a binary word comprising:

a first circuit for decomposing M into two integers A and B, wherein B = M – A;

a second circuit for evaluating C = A modulo J (A mod J);

a third circuit for evaluating M′ = C + B,

a fourth circuit for outputting M′ or feeding M′ back to the first circuit to evaluate M′ modulo J; and

fifth circuit for ensuring convergence comprising a multiplexer (M3) configured to pass J when the bitwise AND of M′ and J equals J and configured to pass 0, otherwise.

22. (New) A system in accordance with claim 21, wherein the output of the multiplexer (M3) is subtracted from M′ by an adder (A2) and the result is passed to the fourth circuit.

23. (New) A system in accordance with claim 21, wherein the second circuit comprises:

a look-up table configured to store $C_i = 2^i$ modulo J for i = 0 to N; and

a multiplexer (M2) configured to pass 0 to the third circuit when ($\alpha_i = 0$), and pass C_i when ($\alpha_i = 1$).